16.2 Fine-Grained In-Circuit Continuous-Time Probing Technique of Dynamic Supply Variations in SoCs

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The design of highly integrated SoCs for consumer electronics faces a great challenge in one-time silicon success with deep sub-100nm CMOS, where the outcome in a short development time must be well-balanced among low power, high performance, and optimum margins against static variability of device properties as well as dynamic variations due to circuit operation. Power supply noise is of prime importance in deciding the best trade-off of circuit performance with design margin for a sufficient yield. This paper reports an in-circuit continuous-time power-supply-voltage probing technique for visualization of circuit-wide noise distribution at a high granularity of the cell-row level, as well as its response to dynamic operation-mode transitions. A practical use of the on-chip noise monitoring technique in a densely integrated digital circuit is demonstrated by fine-pitch placements and routing of in-circuit detectors and gain-calibrated continuous-time analog waveform acquisition.

Figure 16.2.1 illustrates an SoC that incorporates a 32b RISC microprocessor (CPU core), a program memory with controller (MC), instruction-cache (I-cache) and data-cache (D-cache) memories, and PLL. The CPU core, MC, and caches have individual supply (V_{DD}) and ground (Gnd) meshes that are commonly tied to wide vertical trunks located on both the left and right sides of the processor. Four pairs of V_{DD} and Gnd pads are allocated and connected to the trunks for power supply. The built-in probing (BP) circuit arrays of Fig. 16.2.2 are located in the left, center, and right of the CPU core. High-precision (HP) on-chip waveform monitors are arrayed in the outside of the CPU core, and their probe wirings are drawn to V_{DD} and Gnd wires around numbered positions from #1 to #13 of Fig. 16.2.1. Figure 16.2.7 shows the die micrograph of the SoC testchip manufactured in STARC 90nm CMOS. The CPU core is based on an M32R architecture and has fully synthesizable internal modules of a memory interface (CIFTOP), a data-path unit (HCPU), and a control unit (CPUCNT).

Built-in probing (BP) circuits, shown in Fig. 16.2.2, use 1.0V transistors with minimum gate length. NMOS and PMOS BP circuits sense voltages on adjacent power supply wirings at a nominal V_{DD} of 1.0V and Gnd of 0.0V and transform a change in voltage into current that flows to a current mirror (CM) for read out. Each BP circuit has a source follower for voltage sensing and a common-source amplifier for current conversion and the capability of selective capture by a scan chain. All BP circuits other than the one selected are fully cut off. The BP circuit eliminates the S/H function of [1] and works in a continuous-time manner with an off-chip oscilloscope for digitizing the output from CM. The symmetrical design of complementary NMOS and PMOS BP circuits allows their read-out CM branches to share a single pad. One of the CM branches is exclusively turned on in relation to the selection of a BP circuit. Finally, the compactness of the entire array allows for wide-bandwidth, fine-grained in-circuit analog waveform acquisition. Post-layout simulation shows an AC bandwidth of 1.2GHz and a large-signal input range of 300mV. The current draw of a BP circuit is 2mA, and that of the CM is 8mA when driving a 50Ω off-chip termination resistor. A BP circuit is formed with deep N-well isolation to avoid interference from surrounding digital circuits, and has a core area of $30.0\times12.6\mu m^2$ that is fitted to 5 cell rows with 2.52μm pitch in a 90nm CMOS standard-cell based layout. Each BP array includes two sets of 20 BP circuits equally shared for V_{DD} and Gnd monitoring and connected to a single CM circuit. A total of 120 BP circuits are distributed throughout the CPU core.

A high-precision (HP) on-chip waveform monitor, based on [2], operates in sample/hold and digitization at the resolution of 800μV and 100ps. The high linearity of the HP monitor up to 600mV input range is confirmed in the gain calibration with external reference signals (EXT) and used to calibrate BP circuits. The HP monitor is necessary to probe the inside of fixed hardwired designs such as SRAM cores in which BP circuits cannot be placed, however, the large area penalty prevents its use for high-density in-circuit probing. The HP monitor probe wirings to distant measurement points shown in Fig. 16.2.1 are routed through the power-supply meshes in the highest layer metal.

Dynamic V_{DD}- and Gnd-voltage variation is induced by CPU operation and also strongly altered when the operation-mode of the CPU is dynamically transitioned. Figure 16.2.3 shows waveforms measured by BP circuits when the CPU starts to access I- and D-caches. Expanded waveforms are consistent among the BP circuit and HP monitor and distinctly characterized by regular peak drops with the interval of clock cycles at 300 MHz. Figure 16.2.4 compares a distribution of peak-to-peak variation (V_{pp}) in V_{DD} and Gnd waveforms at local supply wirings when I-/D-caches are activated and deactivated, where the cache operation is controlled with a test vector. The dots represent waveforms measured by the BP circuit and the crosses are measured by the HP monitor. The numbers in the *x*-axis correspond to the HP probe points and serve as a marker of measurement locations shown in Fig. 16.2.1. The higher activity in SRAM cores in a cache-on state enlarges dynamic voltage variations. Note that the increase in V_{pp} substantially differs between V_{DD} and Gnd, which requires careful assessment for noise margins due to asymmetric variability among rise and fall logic path delays. This observation is only achieved with the externally referenced separate measurements on V_{DD} and Gnd, and not by effective-supply voltage measurements [3]. The V_{pp} distribution is roughly higher in the left and lower in the right. This reflects the higher noise generation in MC and CIFTOP due to intensive logic operations in exchanging binary data with SRAM cells. In-circuit probing of the 120 locations interpolates the high-precision measurements and shows the dependence of dynamic noise on the distribution of logic activity as well as power-supply impedance. These on-chip observations, which have never been achieved by coarse monitor locations in prior arts [2-4], are a practical method to validate a design flow for integrity.

Figure 16.2.5 shows V_{DD} and Gnd waveforms continuously measured by a BP circuit, during 5× frequency-hopping operations at 350MHz. Again, the waveforms of the BP circuit and HP monitor are consistent. The transition of voltage variations clearly reflects an immediate change in clock frequencies as well as long-term damping. Figure 16.2.6 illustrates the transition of dynamic voltage drop (V_{pp}) during the frequency hopping, comparing 2× and 5× frequency differences. The largest V_{pp} occurs in the CPU in the intermediate state of 5× frequency hopping, and then V_{pp} settles in the final state. The excessive V_{pp} transition leads to erroneous operations. In-circuit continuous and highly distributed measurements can explain their cause in terms of local and global supply integrity.

Acknowledgment:
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References:
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[2] M. Nagata, J. Nagai, T. Morie, and A. Iwata, "Measurements and Analyses of Substrate Noise Waveform in Mixed-Signal IC Environment," *IEEE Trans. Comput.-Aided Des. Integrat. Circuits Syst.*, vol. 19, no. 6, pp. 671-678, Jun., 2000.
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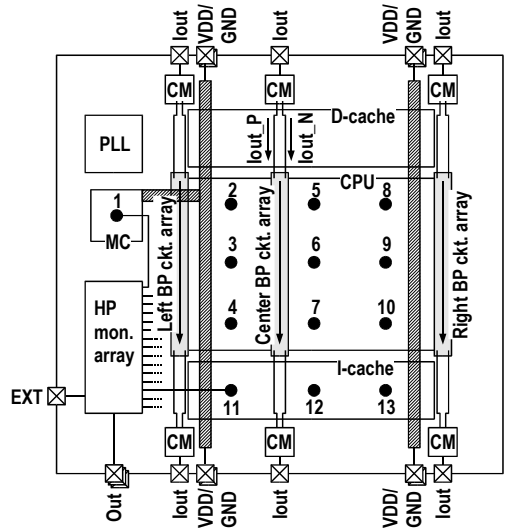

Figure 16.2.1: An SoC featuring built-in probing (BP) circuit arrays and high-precision (HP) monitor arrays.

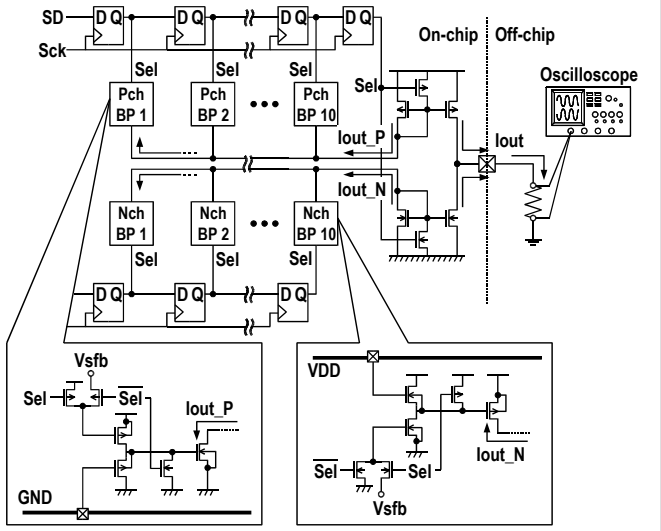

Figure 16.2.2: Schematic diagram of built-in probing circuit array and read-out current mirror.

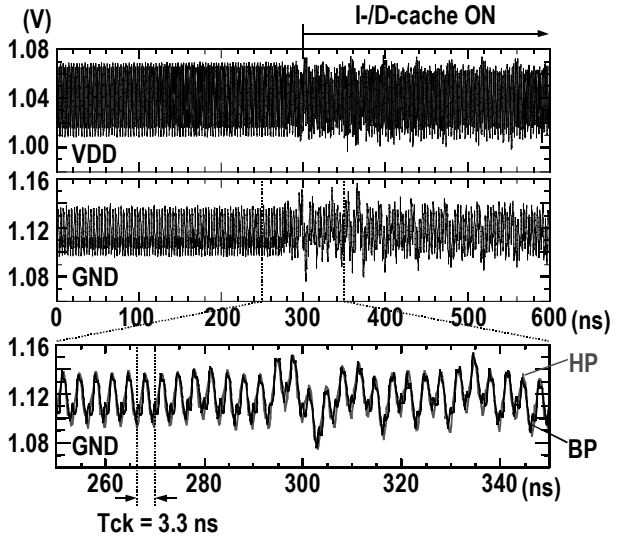

Figure 16.2.3: Measured power supply (V_{DD}) and ground (Gnd) waveforms when I-/D-cache memories start to activate in a CPU core.

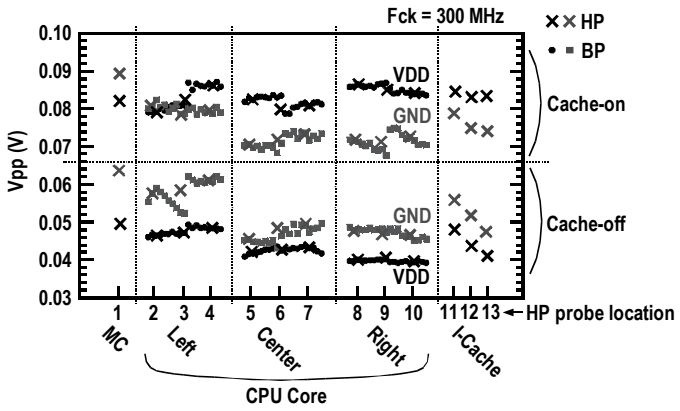

Figure 16.2.4: Peak-to-peak change in voltage (V_{pp}) distribution in an entire chip, comparing cache-on and cache-off states.

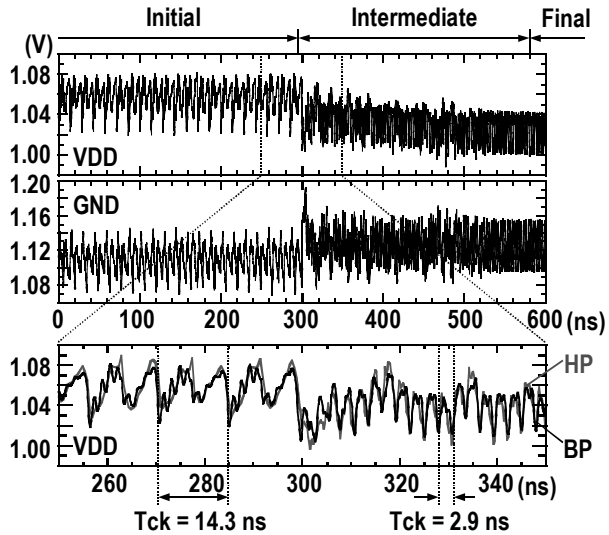

Figure 16.2.5: Measured power supply (V_{DD}) and ground (Gnd) waveforms when operating clock frequency is hopping from 70 MHz to 350 MHz.

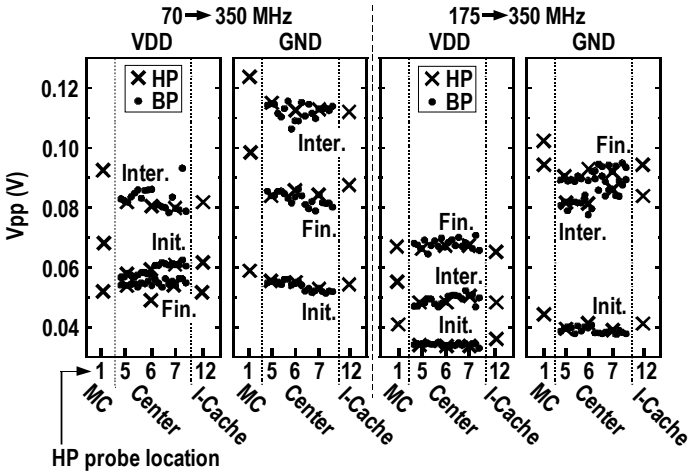

Figure 16.2.6: Peak-to-peak change in voltage (V_{pp}) distributions in an entire chip for initial, intermediate, and final states during operating clock frequency hopping. Frequency transitions from 70 to 350MHz (5x) and 175 to 350MHz (2x) are compared.

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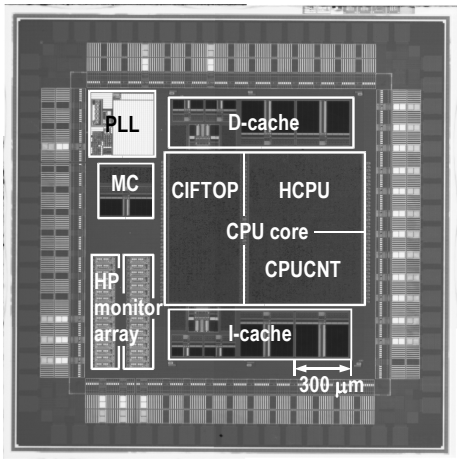

- Technology
  - 90 nm CMOS
    1.0 V, 6 LM, Triple well
- Chip size
  2.5 mm x 2.5 mm
- Contents
  - 32-bit RISC CPU core
  - I-cache: 8 KB
  - D-cache: 8 KB
  - Program(MC): 2 KB
  - BP array/HP array
- Transistor count
  - 700 K

Figure 16.2.7: Chip micrograph.

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